Jitter Effects On 100BASE-T Timing

Time Interval Error Detects Excessive Phase Jitter

Jitter, the variation of circuit timing from expected values, can cause major problems in data communications systems.

Consider the block diagram of the physical layer interface for a 100Base-T ethernet shown in figure 1. The quality of the 50 MHz clock has a major effect on the correct operation of the system. In many cases a simple measurement of clock frequency does not reveal any problem, but a closer look at the phase or time interval jitter reveals major difficulties.

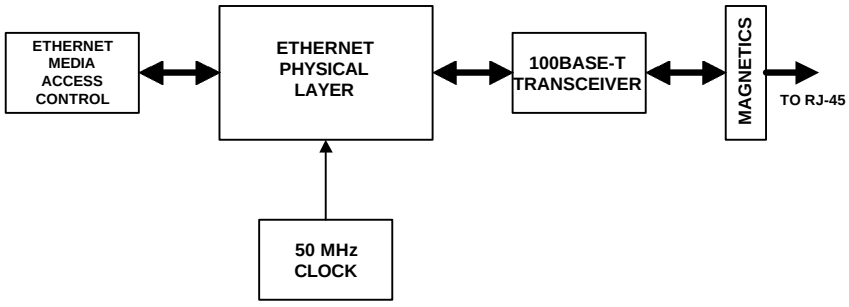

Figure 1 – Excessive clock jitter can cause missed data packets in Ethernet local area networks

LeCroy's implementation of the Time Interval Error (TIE) JitterTrack function, shown in figure 2, measures the actual locations of a selected clock edge against an ideal location based on a user specified clock frequency. When applied to a uniform clock waveform the time interval error measures the instantaneous phase variation of the clock on a cycle by cycle basis. Even if the average frequency of the clock is constant there can be large variations in phase. These variations can cause major timing errors as can be seen in the following example

LeCroy designers of a 100 Base-T ethernet interface made some unrelated circuit changes in the system processor and suddenly began to notice that packets were being missed. A measurement of the 50 MHz oscillator frequency and the 25 MHz transmit (Tx) clock did not reveal any change. The 50 MHz oscillator was a phase locked loop (PLL) based device which did not have a jitter specification. Looking at the clock signal with analog persistence led the engineer to suspect that this oscillator was the source of the problem. Subsequent measurements using TIE quantified the jitter. The designers replaced the PLL with a crystal oscillator and the problem disappeared.

The TIE measurements were made using LeCroy's Jitter and Timing Analysis option. In figure 3 the performance of the crystal

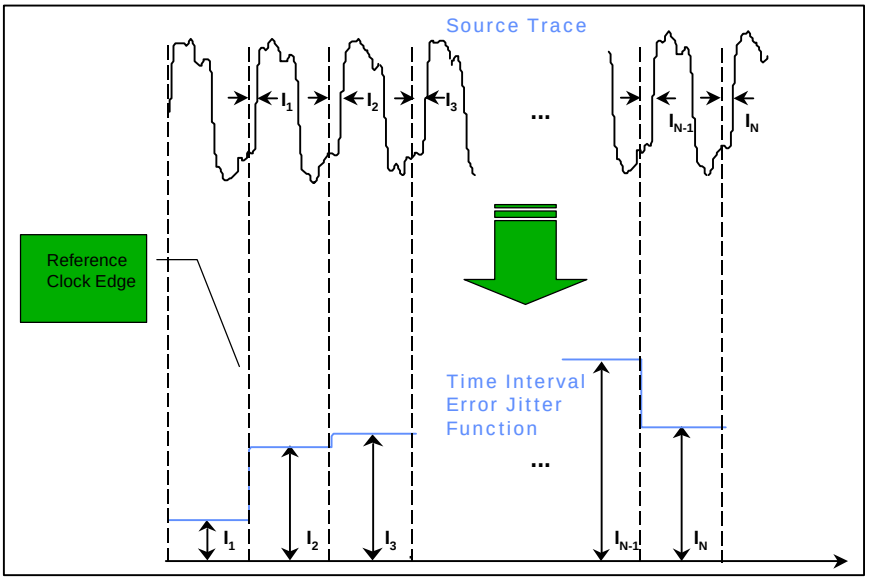

Figure 2- The Time Interval Error (TIE) JitterTrack function

oscillator is shown.

The acquired clock shown in the top waveform (channel 2). Time interval error (trace A) and cycle to cycle period jitter (trace B) are computed for 1 ms (50,000 cycles) of the 50 MHz clock. In addition the histogram of the time interval error at level (tie@lv) parameter is shown in trace C. The histogram parameters avg, sigma and range read the mean, standard deviation or rms jitter, and peak to peak jitter of the interval error. Note that the range or peak to peak jitter is 1.553 ns.

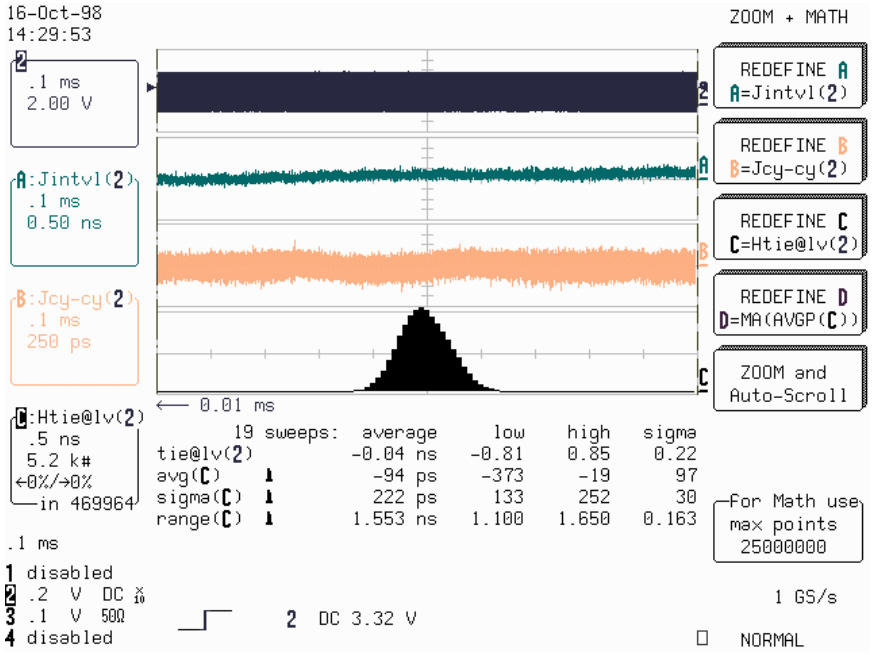

Figure 3 –Time interval error analysis of the working clock oscillator

Compare this value with the jitter analysis of the original 50 MHz PLL based clock shown in figure 4. This is the oscillator associated with the dropped data packets. Note that the cycle to cycle variation in period (trace B) has not changed appreciably. The time interval error function and the related histogram parameters show a large increase in TIE. In particular the peak to peak phase jitter has increased to 12.7 ns

When analyzing timing measurements it is helpful to have access to cycle by cycle analysis of frequency/period, width, duty cycle, time interval error, and cycle to cycle period variation. As can be seen from this example, problems do not necessarily appear in all measurements.

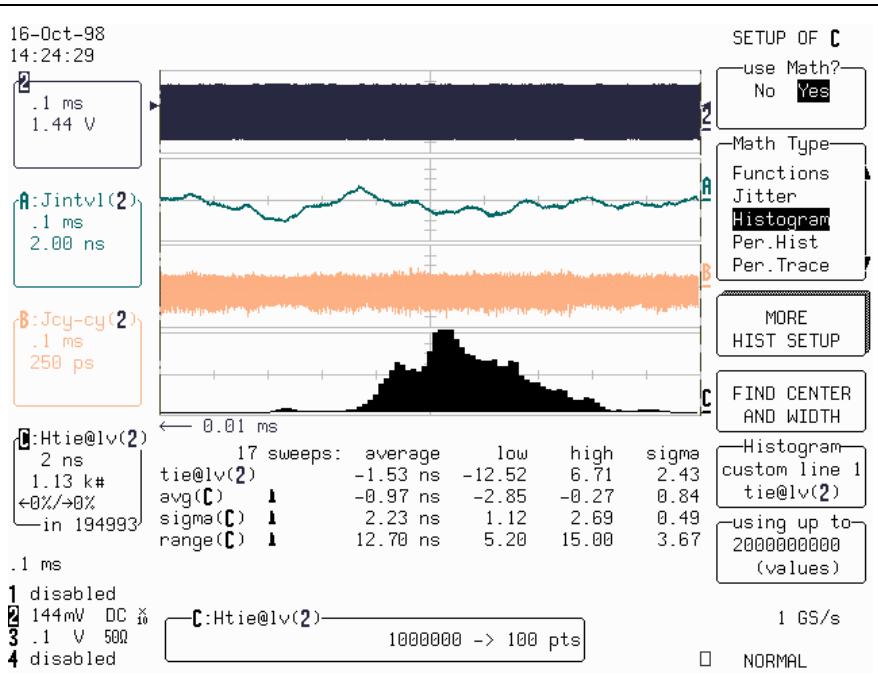

Figure 4 - Time interval error analysis of the PLL clock